IN THE CLAIMS

Claims 19-28 Cancelled.

29. (New) A method of testing multiple integrated circuits simultaneously, the method comprising the steps of:

executing a tester controller program residing in an Automatic Test Equipment (ATE), the tester controller program and ATE having a design intended to test one integrated circuit at a time; and

executing a multi-test program, residing external to the ATE, in conjunction with the tester controller program so that the ATE can test multiple integrated circuits simultaneously.

30. (New) The method of claim 29 further comprising the step of:

creating a multi-test program from generic rules that describe the structure of each of the tests to be applied to each of the integrated circuits, the structure having a description that is independent from any of the integrated circuits.

31. (New) The method of claim 30 wherein the step of creating includes the step of:

creating the multi-test program from pattern data that describes pattern vectors and scan patterns for each of the integrated circuits.

32. (New) The method of claim 31 wherein the step of creating includes the step of:

creating the multi-test program from pin data that describes the ATE pin mappings for each one of the integrated circuits.

33. (New) An apparatus for testing multiple integrated circuits simultaneously, the apparatus comprising:

an Automatic Test Equipment (ATE) having a tester controller program residing therein, the ATE and tester controller program having a design intended to test one integrated circuit at a time; and

a computer, external to the ATE, for executing a multi-test program in conjunction with the tester controller program so that the ATE can test multiple integrated circuits simultaneously.

34. (New) The apparatus of claim 33 further wherein the computer further comprises:

hardware for creating a multi-test program from generic rules that describe the structure of each of the tests to be applied to each of the integrated circuits, the structure having a description that is independent from any of the integrated circuits.

35. (New) The apparatus of claim 34 wherein the hardware includes:

hardware for creating the multi-test program from pattern data that describes pattern vectors and scan patterns for each of the integrated circuits.

36. (New) The apparatus of claim 35 wherein the hardware includes:

hardware for creating the multi-test program from pin data that describes the ATE pin mappings for each one of the integrated circuits.

37. (New) An apparatus for testing multiple integrated circuits simultaneously, the apparatus comprising:

means for executing a tester controller program residing in an Automatic Test Equipment (ATE), the tester controller program and ATE having a design intended to test one integrated circuit at a time; and

means for executing a multi-test program, residing external to the ATE, in conjunction with the tester controller program so that the ATE can test multiple integrated circuits simultaneously.

38. (New) The apparatus of claim 37 further comprising:

means for creating a multi-test program from generic rules that describe the structure of each of the tests to be applied to each of the integrated circuits, the structure having a description that is independent from any of the integrated circuits.

39. (New) The apparatus of claim 38 wherein the means for creating includes:

means for creating the multi-test program from pattern data that describes pattern vectors and scan patterns for each of the integrated circuits.

40. (New) The apparatus of claim 39 wherein the means for creating includes:

means for creating the multi-test program from pin data that describes the ATE pin mappings for each one of the integrated circuits.

CLAIM OBJECTIONS AND REJECTIONS

In the prior Office Action, the Examiner objected and rejected claims 19-28. Claims 19-28 have been cancelled. New claims 29-40 have been added. Applicants' discuss the cited references below to the extent they are applicable to the new claims.

U.S. Patent No. 6557128 B1 to Turnquist ("Turnquist") discloses a ATE that is modified using specialized hardware (pin-unit/system controller interface 32) to allow simultaneous testing of multiple integrated circuits (DUTs) (see Col. 4 lines 23-30 and corresponding Figure 3, Col. 4 lines 44-49). The specialized hardware allows Turnquist to group pins together for virtual testers.

Applicant's present invention, as now defined by the pending claims, in one aspect is a method for testing multiple integrated circuits. The method includes the step of executing a tester controller program residing in an Automatic Test Equipment (ATE), the tester controller program and ATE having a design intended to test one integrated circuit at a time. The method further includes the step of executing a multi-test program, residing external to the ATE, in conjunction with the tester controller program so that the ATE can test multiple integrated circuits simultaneously

In contrast, Turnquist is void of any discussion using using a tester controller program in combination as now claimed by Applicants. As such, Turnquist fails to disclose, teach or suggest whether used alone or in combination with the cited references Applicants' present invention as now defined by the pending claims.